## ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT, OAKLAND UNIVERSITY ECE-2700: Digital Logic Design

#### Student Honor Pledge:

All work submitted is completed by me directly without the use of any unauthorized resources or assistance Initials: \_\_\_\_\_

# Solutions - Quiz 4

(Nov. 30<sup>th</sup> @ 5:30 pm)

### PROBLEM 1 (30 PTS)

- Given the following State Machine Diagram.
  - ✓ Is this a Mealy or a Moore machine? Why?
  - ✓ Provide the <u>State Table</u> and the <u>Excitation Table</u>.
    - Use S0 ( $\overline{Q}$ =00), S1 ( $\overline{Q}$ =01), S2 ( $\overline{Q}$ =10), S3 ( $\overline{Q}$ =11) to encode the states.

X	PRESENT STATE	NEXT STATE	z	PRE x Ç	<b>SE</b> 21Q	MT STATE	<b>N</b> Q <sub>1</sub>	<b>EXTST</b>	ATE 1) z
0	S0	S2	0	0	0	0	1	0	0
0	S1	S1	0	0	0	1	0	1	0
0	S2	S1	0	0	1	0	0	1	0
0	S3	SO	1	0	1	1	0	0	1
1	S0	S1	0	1	0	0	0	1	0
1	S1	S3	0	1	0	1	1	1	0
1	S2	S3	0	1	1	0	1	1	0
1	S3	S2	0	1	1	1	1	0	0



### PROBLEM 2 (40 PTS)

• Complete the timing diagram of the following FSM (represented in ASM form):



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#### PROBLEM 3 (30 PTS)

• Sequence detector: Draw the state diagram (any representation) of an FSM with input x and output z. The detector asserts z = 1 when the sequence 1110 is detected. Right after the sequence is detected, the circuit looks for a new sequence.

